Dynamic Circuit Compilation for Sparse Qubit Connectivity

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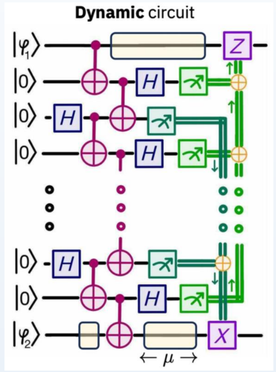
Abstract

In this work, we show how dynamic circuit compilation methods can transform a densely connected circuit into an ancilla-mediated, sparsely connected dynamic circuit that includes mid-circuit measurement and feedforward operations. This sparse connectivity is better suited to current quantum hardware, which often has limited qubit connectivity.

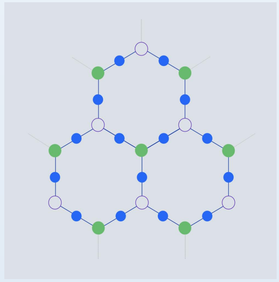
Compared to compilation methods focused on unitary circuits, our method can reduce both circuit depth and the additional CNOTs required to execute non-adjacent qubit interactions.

Introduction



- Dynamic quantum circuits with mid-circuit-measurements and feed-forward operations enable the implementation of long-range entangling gates in **constant depth** with **linear connectivity** [1], [2].

- Many quantum hardware platforms impose connectivity constraints, allowing two-qubit gates only between adjacent qubits.



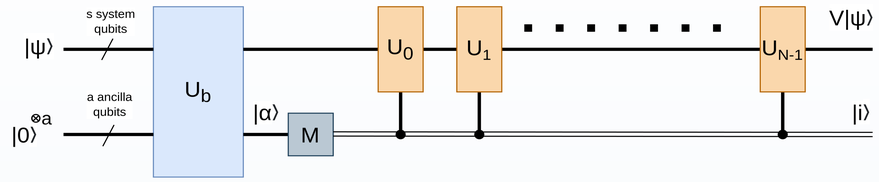
- These qubits are often organized so that a subset of them serve as "**system**" or "**data**" qubits, while the remaining ones act as "**ancillas**", interleaved among the data qubits. Examples include Google's Sycamore chip and IBM's heavy-hex architecture.

- We build on the recently proposed **AC/DC framework [3]**, which enables automated compilation of dynamic circuits for arbitrary unitaries.

- In this work, we explore using dynamic circuits to compile logical circuits that require **dense**, or even **all-to-all connectivity**, into physical circuits executable on hardware with limited connectivity, while reducing the circuit **depth** and additional **number of CNOTs** used.

- While all examples in this poster target linear connectivity, **note that our framework supports arbitrary topologies.**

Methodology



AC/DC protocol of [3] for preparing a target unitary V: Here s denotes the number of system qubits and a denotes ancilla qubits initialized to $|0\rangle^{\otimes a}$. M represents mid-circuit measurements on the ancillas, with $|\alpha\rangle$ and $|i\rangle$ being the pre- and post- measurement states, respectively. U_b is the "base" circuit applied to all the s + a qubits, while each U_i is a "branch" circuit applied conditionally on the measurement outcome $|i\rangle$, for i ∈ {0, 1, ..., N − 1}, N = 2^a .

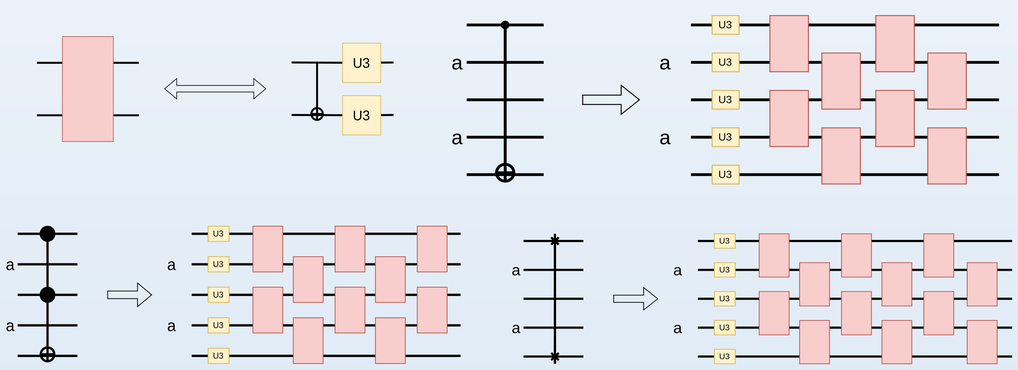
By deferring the measurement to after the branch circuits, we obtain a composite unitary

$$U = (\sum_{i=0}^{N-1} U_i \otimes |i\rangle\langle i|)U_b$$

We treat U_b and the U_is as parameterized ansatzes and optimize their parameters to implement the target unitary V by minimizing the cost function defined in [3]: where $|\alpha\rangle$ is the pre-measurement state of the ancilla qubits.

$$C_{dyn1} = 1 - \frac{1}{2^s}\left|Tr((V \otimes |\alpha\rangle\langle 0|)^\dagger U)\right|$$

Results



Circuit	CNOT Depth		CNOT count	
	Dynamic	Unitary	Dynamic	Unitary
5 qubit CNOT	**4**	13	**8**	19
5 qubit Toffoli	**5**	14	**10**	20
5 qubit SWAP	**6**	15	**12**	21
7 qubit CNOT	**5**	19	**15**	31
7 qubit SWAP	**7**	21	**21**	33

- A red box indicates a layer of CNOT followed by two parameterized U3 gates.

- For the long-range CNOT gate, a U_b ansatz with **just four layers** of nearest-neighbor CNOTs suffices.

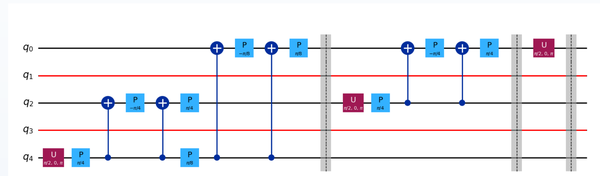
- The Toffoli and SWAP gates require ansatze with just **five and six layers** of CNOTs, respectively.

- A detailed comparison of CNOT counts and depths between dynamic and unitary circuits is shown in the adjacent table

Discussion

- The results shown in the last section enable us to compile circuits that require **dense** or **all-to-all connectivity** into those that can be run on a hardware with **linear nearest-neighbour connectivity**. (Other topologies are also supported.)

- As an example, consider the following circuit, which implements a 3-qubit QFT on a machine with 5 qubits connected in a line.



- The ancilla qubits are marked in red. The logical description of the circuit has CNOTs crossing other qubits which isn't allowed on hardware.

- To compile this circuit, we can use the **dynamic circuits** we constructed in the previous sections implementing **long range CNOT** across five qubits.

- While our method is capable of handling circuits with 7-8 qubits, scaling beyond this remains challenging due to the exponential overhead of optimizing parameterized unitaries with increasing number of qubits.

- However, an important advantage of our approach is that it is **inherently compatible** with the standard qubit mapping/routing techniques of **inserting SWAP gates** to satisfy hardware connectivity requirements

- This opens a promising direction for future work – by combining dynamic circuits with SWAP-based routing, we can develop **hybrid compilation strategies** that scale efficiently to larger and more complex circuits.

References

[1] Bäumer, E., Tripathi, V., Wang, D.S., Rall, P., Chen, E.H., Majumder, S., Seif, A. and Minev, Z.K., 2024. Efficient long-range entanglement using dynamic circuits. PRX Quantum, 5(3), p.030339.

[2] Bäumer, E. and Woerner, S., 2025. Measurement-based long-range entangling gates in constant depth. Physical Review Research, 7(2), p.023120.

[3] Niu, S., Kokcu, E., Mitra, A., Szasz, A., Hashim, A., Kalloor, J., de Jong, W.A., Iancu, C. and Younis, E., 2024. AC/DC: Automated Compilation for Dynamic Circuits. arXiv preprint arXiv:2412.07969.